

**AMENDMENTS TO THE CLAIMS:**

*Please amend the claims as follows:*

1-13. (Cancelled)

14. (Currently amended) A semiconductor device comprising a MOS transistor with a plurality of gate electrodes,

wherein the gate electrodes are formed on a semiconductor substrate having a silicon layer at least in the surface thereof,

the MOS transistor has a gate length of 0.15  $\mu\text{m}$  or smaller and is formed in an element region surrounded with an isolation insulating film,

each of the gate electrodes is arranged between dummy patterns with a space left from each side thereof,

sidewalls are provided on side walls of each of the gate electrodes,

a first silicide layer is formed in the upper portion of the gate electrode,

a second silicide layer is formed in a portion of the semiconductor substrate surface which is located in part of the element region between the gate electrode and the dummy patterns,

the first silicide layer has a greater thickness than the second silicide layer, [[and]]

one of the dummy patterns is a dummy gate electrode which is an electrode pattern having the shape of a gate electrode, and the other dummy pattern is a pattern made of insulating material, and

the dummy patterns are formed on the isolation insulating film.

15. (Previously presented) The device of claim 14, wherein the dummy gate electrode is an electrode which is not electrically connected to a semiconductor integrated circuit of the semiconductor device.

16. (Cancelled)

17. (Previously presented) The device of claim 14, wherein the dummy gate electrode is provided with sidewalls on its side walls and is not electrically connected to a semiconductor integrated circuit of the semiconductor device.

18. (Previously presented) The device of claim 14, wherein the pattern made of insulating material is formed on the isolation insulating film.

19-25. (Cancelled)